

REMARKS

In response to the Office Action mailed January 11, 2005, Applicant has amended claims 1 and 13, requests that claims 15 and 16 be cancelled without prejudice, and submits the following remarks.

Specification

The Patent Office objected to paragraph [0021] of the specification. More specifically, the Patent Office stated that paragraph [0021], lines 16-17 should be amended to fill in the blanks for the application serial number and filing date of the patent application incorporated by reference. Applicant has amended paragraph [0021] accordingly. Thus, the objection to the specification should be withdrawn.

§ 112

The Patent Office rejected claims 6 and 14 under 35 U.S.C. § 112, second paragraph, as being indefinite. More specifically, the Patent Office stated that the meaning of "reproducible termination layer" is unclear. As stated in MPEP § 2173.02, "[d]efiniteness of claim language must be analyzed, not in a vacuum, but in light of: (A) The content of the particular application disclosure; (B) The teachings of the prior art; and (C) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made."

Page 5, lines 24-28 of Applicant's specification states that "[b]y being reproducible, the GaN termination layer 16 may be consistently reproduced each time the HEMT 10 is fabricated." Further, as would be apparent to one of ordinary skill in the art, whether or not the termination layer is consistently reproducible is a function of doping. Thus, for the termination layer to be consistently reproducible, the doping of the termination layer must be consistent each time the manufacturing process is repeated. As such, the language "reproducible termination layer" as used in claims 6 and 14 is definite, and the rejection of claims 6 and 14 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

§ 102

The Patent Office rejected claims 1-3, 5, 9, 11-13, 17-19, and 21 under 35 U.S.C. § 102(b) as being anticipated by Teraguchi (U.S. Patent No. 6,177,685). "A claim is anticipated

only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 UPPQ 2d 1051, 1053 (Fed. Cir. 1987).

Regarding claim 1, Applicant has amended claim 1 to clarify that the sub-buffer layer is adapted to increase a source-drain breakdown voltage of the GaN transistor structure. Teraguchi fails to expressly or inherently disclose a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering the transitional layer and the substrate during high voltage operation. In Figure 7, Teraguchi discloses a buffer layer (32). Regarding the buffer layer (32), in column 7, line 66 – column 8, line 2, Teraguchi states that “in the case of the HFET structure formed on the undoped AlN buffer layer, a flow of carriers into the substrate does not occur, so that the electron mobility is increases.” (emphasis added). However, Teraguchi fails to disclose that the AlN buffer layer operates to increase a source-drain breakdown voltage of the GaN transistor structure. Further, increasing the source-drain breakdown voltage is not inherent in the structure of Teraguchi. As discussed in MPEP § 2112, to be “inherent”, there must be a basis in technical fact or reasoning to reasonably support the determination that that characteristic “necessarily flows from the teachings of the applied prior art.” *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. (1990) (emphasis in original). Further, as would be apparent to one of ordinary skill in the art, increasing the electron mobility does not necessarily increase the source-drain breakdown voltage. As such, Teraguchi fails to expressly or inherently disclose a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering the transitional layer and the substrate during high voltage operation. Thus, claim 1 is allowable over Teraguchi.

For at least the same reason claim 1 is allowable over Teraguchi, claims 2, 3, 5, 9, 11, and 12 are allowable. However, Applicant reserves the right to further address the rejection of claims 2, 3, 5, 9, 11, and 12 in the future if necessary.

Regarding claim 13, Applicant has amended claim 13 to include the subject matter from original claims 15 and 16 and requests that claims 15 and 16 be cancelled without prejudice. Since original claims 15 and 16 were not rejected under 35 U.S.C. § 102(b) as being anticipated by Teraguchi, amended claim 13 is allowable over Teraguchi.

§ 103(a) – Yu and Teraguchi

The Patent Office rejected claims 1-5, 7-13, and 15-21 under 35 U.S.C. § 103(a) as being unpatentable over Yu (U.S. Patent No. 6,624,452) in view of Teraguchi (U.S. Patent No. 6,177,685). In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. According to MPEP 2143.03, “[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.”

Regarding claim 1, the combination of Yu and Teraguchi fails to teach or suggest at least a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering the transitional layer and the substrate during high voltage operation. As discussed above, Teraguchi teaches an undoped AlN buffer layer that stops the flow of carriers into the substrate so that the electron mobility is increased. However, Teraguchi fails to teach or suggest that the AlN buffer layer operates to increase a source-drain breakdown voltage of the GaN transistor structure. Yu fails to correct this deficiency. As admitted by the Patent Office, Yu fails to teach the claimed sub-buffer layer. As such, Yu also fails to teach or suggest the claimed sub-buffer layer that is adapted to increase a source-drain breakdown voltage of the GaN transistor structure. Since the combination of Yu and Teraguchi fails to teach or suggest at least a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering the transitional layer and the substrate during high voltage operation, claim 1 is allowable over the combination of Yu and Teraguchi.

For at least the same reasons claim 1 is allowable over the combination of Yu and Teraguchi, claims 2-5 and 7-12 are also allowable. However, Applicant reserves the right to further address the rejections of these claims in the future if necessary.

Regarding amended claim 13, the combination of Yu and Teraguchi fails to teach or suggest the claimed GaN termination layer, wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer and is approximately 1-2 nanometers (nm) thick. The Patent Office states that Yu discloses a GaN termination layer that is approximately 10 nanometers (nm) thick that is sufficiently thin to allow electrons to tunnel through the GaN termination layer. The Patent Office further states that the rejection is proper even though the claimed range and the prior art range do not overlap because one skilled in the

art would have expected them to have the same properties. Applicant respectfully disagrees. The claimed 1-2 nm thickness is 5 -10 times smaller than the 10 nm thickness disclosed by Yu. It would be apparent to one of ordinary skill in the art that the properties of a 10 nm thick GaN layer are significantly different than the properties of a 1-2 nm thick GaN layer with respect to electron tunneling. As such, Yu fails to teach or suggest a 1-2 nm thick GaN termination layer. Since the combination of Yu and Teraguchi fails to correct this deficiency, claim 13 is allowable.

For at least the same reasons claim 13 is allowable over the combination of Yu and Teraguchi, claims 17-21 are also allowable. However, Applicant reserves the right to further address the rejections of claims 17-21 in the future if necessary.

§ 103(a) – Micovic and Teraguchi

The Patent Office rejected claims 1-5, 7-13, and 15-21 under 35 U.S.C. § 103(a) as being unpatentable over Micovic (U.S. Publication No. 2003/0218183) in view of Teraguchi (U.S. Patent No. 6,177,685). In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. According to MPEP 2143.03, “[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.”

Regarding claim 1, the combination of Micovic and Teraguchi fails to teach or suggest at least a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering the transitional layer and the substrate during high voltage operation. As discussed above, Teraguchi teaches an undoped AlN buffer layer that stops the flow of carriers into the substrate so that the electron mobility is increased. However, Teraguchi fails to teach or suggest that the AlN buffer layer operates to increase a source-drain breakdown voltage of the GaN transistor structure. Micovic fails to correct this deficiency. As admitted by the Patent Office, Micovic fails to teach the claimed sub-buffer layer. As such, Micovic also fails to teach or suggest the claimed sub-buffer layer that is adapted to increase a source-drain breakdown voltage of the GaN transistor structure. Since the combination of Micovic and Teraguchi fails to teach or suggest at least a sub-buffer layer deposited above the transitional layer and adapted to increase a source-drain breakdown voltage of the GaN transistor structure by preventing electrons from entering

the transitional layer and the substrate during high voltage operation, claim 1 is allowable over the combination of Micovic and Teraguchi.

For at least the same reasons claim 1 is allowable over the combination of Micovic and Teraguchi, claims 2-5 and 7-12 are also allowable. However, Applicant reserves the right to further address the rejections of these claims in the future if necessary.

Regarding amended claim 13, the combination of Micovic and Teraguchi fails to teach or suggest the claimed GaN termination layer, wherein the GaN termination layer is sufficiently thin to allow electrons to tunnel through the GaN termination layer and is approximately 1-2 nanometers (nm) thick. The Patent Office states that Micovic discloses a GaN termination layer that is approximately 5 nanometers (nm) thick that is sufficiently thin to allow electrons to tunnel through the GaN termination layer. The Patent Office further states that the rejection is proper even though the claimed range and the prior art range do not overlap because one skilled in the art would have expected them to have the same properties. Applicant respectfully disagrees. The claimed 1-2 nm thickness is 2.5 - 5 times smaller than the 5 nm thickness disclosed by Micovic. It would be apparent to one of ordinary skill in the art that the properties of a 5 nm thick GaN layer are significantly different than the properties of a 1-2 nm thick GaN layer with respect to electron tunneling. As such, Micovic fails to teach or suggest a 1-2 nm thick GaN termination layer. Since the combination of Yu and Teraguchi fails to correct this deficiency, claim 13 is allowable.

For at least the same reasons claim 13 is allowable over the combination of Micovic and Teraguchi, claims 17-21 are also allowable. However, Applicant reserves the right to further address the rejections of claims 17-21 in the future if necessary.

Conclusion

In view of the discussion above, claims 1-14 and 17-21 are allowable. Reconsideration is respectfully requested. If any issues remain, the examiner is encouraged to contact the undersigned attorney of record to expedite allowance and issue.

Respectfully submitted,

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